**Pre-Lab:**

1. Design a CB stage with a voltage gain of 10 and an input impedance of 50 Ohms. The biasing should be of the voltage divider type with a bypass capacitor attached to the base.
2. Find the output impedance of the CB stage.
3. Design an Emitter follower for a load resistance of 10 Ohms and a gain of 0.9.
4. Find the input and the output impedance of the Emitter follower.

**Lab Tasks:**

Task #1:

1. Implement the CB stage in the prelab using LTspice netlist. Assume that the CB stage is loaded with a 100 KOhms resistance. Couple the input and the output using 1 mF capacitors. The input is a 1 mV signal with a 500 Hz frequency.
2. Perform a transient analysis for step “a” and plot the input and the output voltages. Observe the gain and the phase relationships. Justify your observation theoretically and mathematically.
3. Observe the input and the output currents. Justify the observed gain theoretically and mathematically.
4. Connect a load resistance of 10 Ohms to the CB stage and observe the effects on the gain. Justify your observation. Suggest a solution to address this problem.
5. Using the netlist capabilities find the input and the output impedance. (Refer to Lab 7 in EENG 330). Verify that the measured values = the theoretical values.

Task #2:

1. Assuming the output voltage of the CB stage to be the input voltage for the EF stage, write a netlist that implement the EF stage in the pre-lab. Use a 1mF capacitor to couple the input to the EF stage.
2. Plot the input and output voltages and observe the gain and the phase shift. Justify your observation using theory and mathematical formulation. You may need to plot the input and the output on separate plots as the output will have a DC offset which will eventually reduce the visibility of the circuit effects.
3. Using the netlist command, find the input and the output impedances. Justify your answers.

Task #3:

1. Connect the CB stage in series to the EF stage. This kind of connections is called cascading. Feed the input voltage to the CB stage and extract the output from the EF stage. Plot the input and the output voltages. Observe the gain and the phase shift.
2. To justify your observations theoretically you need to be aware of the effects of cascading on amplifiers. The following schematic should help you understand how to perform the analysis:

